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AGILENT TECHNOLOGIES
Legal Departmet, 51U-PD
Intellectual Property Administration
P.O. Box 58043
Santa Clara, CA 95052-8043

EXAMINER	
AGGARWAL, YOGESH K	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/827,942	MENTZER, RAY ALAN	
	Examiner	Art Unit	
	Yogesh K Aggarwal	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments filed 11/10/2004 have been fully considered but they are not persuasive.

Examiner's response:

2. Applicant argues w.r.t amended claims 1, 9 and 17 that Dolazza (US Patent # 4,573,035) teaches that the same stabilized sample signal from the A/DC 280 is used to produce the +Ref and -Ref signals and to digitize an analog signal, i.e. the stabilizing sample signal to derive a digitized signal. Consequently, the +Ref and -Ref signals cannot be based on an image signal of a previously processed pixel while the digitized signal is derived from analog signal of a current pixel. Therefore Dolazza does not describe, teach or suggest the element of providing a high signal and a low signal based on an image signal of a previously processed pixel as recited in the amended claim 1. The Examiner respectfully disagrees. The analog signal V that is received by the S/H 280 is used to generate a stabilized sample of V. This stabilized value V is input to A/DC converter 282 to generate a first digitized word. This is further input to a Programmable Read only memory (PROM) 284, which stores the first word and generates +Ref and –Ref analog signals after inputting through DACs 286 and 288. The +Ref and –Ref analog signals so generated are used to digitize a stabilized value of the analog signal V. This is true for first analog signal. The subsequent values of stabilized sample V (output of element 280) that is input to the A/DC 290 is digitized by the +Ref and –Ref already generated. As Dolazza states in col. 10 lines 22-30,

The upper analog signal and the lower analog signal is received by A/DC 290 as external upper and lower reference signals respectively, **which permit the A/DC to convert the analog signal from S/H 280 to a digital output signal** along a piece-wise linear transformation curve

(approximately curve 268 of FIG. 6) having 64 linear segments corresponding to the 6 bit value of the first digital word (2.sup.6 =64).

Therefore the current value of analog signal from S/H 280 is converted to a digital output based on the upper and lower reference signals respectively, which are only generated once. If the values of +Ref and –Ref are generated for each pixel, the time to digitize all pixels will be large. Assuming 1 million pixels and 1 microsecond clock pulse, the time it will take to generate +Ref and –Ref will be 1 second (assuming 1 clock pulse for each generation) for the whole operation or if the whole operation is made parallel the size of the circuit is large. Therefore the values of upper and lower signals are based upon previously processed pixels while the digitized signal is derived from analog signal of a current pixel.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim1-3, 9, 10 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Dolazza (US Patent # 4,573,035).

[Claim 1]

Dolazza teaches a method of correcting erroneous image signals (col. 10 lines 31-40) comprising providing a high signal and a low signal (figure 7, +Ref and –Ref) based on an image signal of a previously processed pixel [The +Ref and –Ref analog signals so generated are used to digitize a stabilized value of the analog signal V. This is true for first analog signal. The subsequent values of stabilized sample V (output of element 280) that is input to the A/DC 290 is digitized by the

+Ref and –Ref already generated. Therefore the current value of analog signal from S/H 280 is converted to a digital output based on the upper and lower reference signals respectively, which are only generated once], said high signal and said low signal defining a signal range about said image signal of said previously processed pixel (+Ref and –Ref define a range); and digitizing an analog signal of a current pixel using said high and low signals as references to derive a digitized signal of said current pixel (output of S/H 280) within said signal range, including limiting said analog signal of said current pixel by said high and low signals (col. 10 lines 22-30).

[Claim 2]

Dolazza teaches a step of converting said image signal of said previously processed pixel to said high signal and said low signal (figure 7, +Ref and –Ref).

[Claim 3]

Dolazza teaches wherein said step of converting said image signal of said previously processed pixel includes digital-to-analog converting (figure 7, 286 and 290) said image signal of said previously processed pixel to said high signal and said low signal (figure 7, +Ref and –Ref), wherein said high and low signals are generated as voltages.

[Claims 9, 10]

These are apparatus claims corresponding to method claims 1 and 3 respectively. Therefore they have been analyzed and rejected based upon method claims 1, 3.

[Claim 17]

Dolazza teaches a method of correcting erroneous image signals (col. 10 lines 31-40) during analog-to-digital conversion comprising a sensor array of photosensitive pixels (figure 1, element 114), each of said photosensitive pixels being configured to accumulate an analog image signal

when exposed to light (col. 5 lines 60-65) and an analog-to-digital converter unit (figure 1, element 125) operatively coupled to said sensor array to receive analog image signals from said photosensitive pixels, said analog-to-digital converter unit comprising a digital-to-analog converter (figure 286 and 288) that outputs a high signal and a low signal (figure 7, +Ref and –Ref) based on an image signal of a previously processed pixel [The +Ref and –Ref analog signals so generated are used to digitize a stabilized value of the analog signal V. This is true for first analog signal. The subsequent values of stabilized sample V (output of element 280) that is input to the A/DC 290 is digitized by the +Ref and –Ref already generated. Therefore the current value of analog signal from S/H 280 is converted to a digital output based on the upper and lower reference signals respectively, which are only generated once], said high signal and said low signal defining a signal range about said image signal of said previously processed pixel (+Ref and –Ref define a range); and

An analog-to-digital converter (figure 7, element 290) having a high reference input and a low reference input to receive said high signal and said low signal (+Ref and –Ref), said analog-to digital converter being configured to digitize an analog signal of a current pixel (output of block 280) using said high and low signals as references to derive a digitized signal of said current pixel within said signal range, including limiting said analog signal of said current pixel by said high and low signals (col. 10 lines 22-30, figure 7).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6, 16 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dolazza (US Patent # 4,573,035).

[Claim 6]

Dolazza is silent as to the type of analog-to-digital converter, however Official notice is taken of the fact that it is notoriously common to have a flash analog-to-digital converter be used for digitizing a current pixel in order to make the overall process faster. Therefore taking the combined teachings of Dolazza and Official notice, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have flash analog-to-digital converter be used for digitizing a current pixel. The benefit of doing so would be because flash A/Ds have high input bandwidth and very high speeds in the 1 to 4-Gsample/s range.

[Claim16]

This is an apparatus claim corresponding to method claim 6. Therefore it has been analyzed and rejected based upon method claim 6.

[Claim 21]

This claim is substantially similar to claim 16. Therefore it has been analyzed and rejected based upon claim 16.

7. Claims 4, 5, 8, 11-14, 18,19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dolazza (US Patent # 4,573,035) in view of Kim (US Patent # 6,587,144).

[Claims 4 and 5]

Dolazza teaches the limitations of claim 1 but fails to teach ".... Wherein a step of comparing said analog signal of said current pixel with an analog signal of a previously processed pixel and

further comprising a step of converting said image signal of said previously processed pixel to said high signal and said low signal, wherein said high and low signals are dependent on said comparing of said analog signal of said current pixel with said analog signal of said previously processed pixel". However Kim teaches comparing (figure 1, element 42) a present black level signal (read as current pixel signal value) and a preset black reference value (read as previously processed pixel value) to up or down values so that the DC voltage level of the signal is adjusted (col. 2 lines 12-23)[DC voltage ca be either high or low and therefore can be read as high and low signals which are dependent on the comparison between a present black level and preset black reference value]. Therefore taking the combined teachings of Dolazza and Kim, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have comparing said analog signal of said current pixel with an analog signal of a previously processed pixel and further comprising a step of converting said image signal of said previously processed pixel to said high signal and said low signal, wherein said high and low signals are dependent on said comparing of said analog signal of said current pixel with said analog signal of said previously processed pixel. The benefit of doing so would be to correct the black level due to an incorrect pixel as taught in Kim (col. 2 lines 20-21).

[Claim 8]

Dolazza teaches wherein said image signal of said previously processed pixel is a digital signal (output of element 282 in figure 7) but fails to teach "...., wherein said image signal has more bits than said digitized signal of said current pixel". However Kim teaches that the A/d converter output has 10 bits as compared to a 6-bit black level reference value (col. 4 lines 25-30). Therefore taking the combined teachings of Dolazza and Kim, it would have been obvious to one

skilled in the art at the time of the invention to have been motivated to have an image signal having more bits than said digitized signal of said current pixel. The benefit of doing so would be to vary the black reference value as needed as taught in Kim (col. 4 lines 25-26).

[Claim 11]

This is an apparatus claim corresponding to method claim 8. Therefore it has been analyzed and rejected based upon method claim 8.

[Claim 12]

Dolazza teaches a six bit D/A and A/d converter but does not disclose a 10 bit D/A and 7 bit A/D converter. However Official notice is taken of the fact that a 10 bit D/A and 7 bit A/D converter is well known in the art in order to have more sensitivity. Therefore taking the combined teachings of Dolazza, Kim and Official notice, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have used a seven-bit value. The benefit of doing so would be to have a circuit, which has high sensitivity.

[Claim 13]

This is an apparatus claim corresponding to method claims 4 and 5. Therefore it has been analyzed and rejected based upon method claims 4 and 5.

[Claim 14]

Claim 14 recites what was discussed with respect to claim 12.

[Claim 18]

This claim is substantially similar to claim 11. Therefore it has been analyzed and rejected based upon claim 11.

[Claim 19]

This claim is substantially similar to claim 13. Therefore it has been analyzed and rejected based upon claim 13.

8. Claims 7, 15, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dolazza (US Patent # 4,573,035) in view of Embler (US Patent # 6,654,054).

[Claim 7]

Dolazza teaches that the digitized signal is based upon the previously processed pixel as discussed in claim 1 but fails to teach ".... a step of adding a conversion signal to said digitized signal of said current pixel". However Embler teaches that an anti-noise signal is added to the digital signal (col. 11 lines 32-38). Therefore taking the combined teachings of Dolazza and Embler, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have a step of adding a conversion signal to said digitized signal of said current pixel. The benefit of doing so would be to ensure an appropriate that an appropriate noise signal is cancelled as taught in Embler (col. 11 lines 32-38).

[Claim 15]

This is an apparatus claim corresponding to method claim 7. Therefore it has been analyzed and rejected based upon method claim 7.

[Claim 20]

This claim is substantially similar to claim 15. Therefore it has been analyzed and rejected based upon claim 15.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K Aggarwal whose telephone number is (571) 272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, James Groody can be reached on (571) 272-7950. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YKA

TUAN HO
PRIMARY EXAMINER